REMARKS

Applicants appreciate the continued thorough examination of the present application that is reflected in the Official Action of October 7, 2004. Applicants also appreciate the Examiner's indication that Claims 1-20 and 28 are allowed, and that Claims 26 and 27 would be allowable if rewritten in independent form. It would be relatively simple to cancel rejected Claims 21-25 and rewrite claims 26 and 27 in independent form to place the application in condition for allowance. However, after careful study, Applicants have not done so because Applicants respectfully submit that Claims 21-25 are patentable over U.S. Patent 6,122,274 to Kumar for at least the reasons that now will be described. Accordingly, Applicants respectfully request reconsideration of the rejection of Claims 21-25 and allowance of the present application.

In particular, Claim 21 recites:

> 21. An integrated circuit First-In-First-Out (FIFO) memory device comprising:
> a FIFO memory;
> a data input port;
> a data output port;
> a FIFO controller that is configured to operate the FIFO memory as <u>from one up to a predetermined number greater than one of independent FIFO queues</u>;
> a data input system that is configured to write input data from the input port into a first selected one of the independent FIFO queues; and
> a data output system that is configured to read data from a second selected one of the independent FIFO queues. (Emphasis added.)

As shown above, Claim 21 recites that the FIFO controller is configured to operate the FIFO memory <u>from one up to a predetermined number greater than one of independent FIFO queues</u>. For example, as noted in the present application at Page 2, lines 19-21:

> Accordingly, in a single integrated circuit chip, anywhere between one and the predetermined number, such as up to 32 or more, of discrete FIFO queues can be set up.

In sharp contrast, Figure 2 of Kumar, and the accompanying description at Column 6, line 33-Column 8, line 8, describes an ATM switch with decentralized pipeline control having a <u>fixed number</u> **m** of memory modules $\mathbf{40_1}$-$\mathbf{40_m}$. Accordingly, the above-quoted recitation of Claim 21 is simply not described or suggested in Kumar.

The other portions of Kumar cited by the Official Action, in the last lines of Page 2, also do not describe a FIFO memory that is operable as from one up to a predetermined

number greater than one of independent FIFO queues. More specifically, Kumar Column 14, line 64-Column 15, line 23 states:

> The disclosed switching apparatus can employ both single port or dual port memory modules. Use of dual port memory modules enhances the effective memory speed for read and write of ATM cells, and overall switching speed of the disclosed switching apparatus. Use of dual port memory will allow simultaneous WRITE and READ of ATM cells to and from a memory module in the same switch cycle only if WRITE and READ operations do not access same memory location. According to the disclosed switching method of the present invention, the parameter assignment phase ensures that WRITE and READ of ATM cells do not access same memory location of a given memory module. Hence the disclosed switching method makes it possible to use the dual port memory modules for the switching apparatus of the present invention. The WRITE and READ operations (FIG. 8) performed by the memory controllers, can be used for both the single port and dual port memory modules. In case of the use of dual port memory modules, the memory controllers will need to produce write address as well as the read address for their memory modules in the same cycle. The order of WRITE and READ operations performed by the memory controllers (FIG. 8) in a given cycle, to produce write and read addresses, does not matter as the operations performed in either order produce the same final result. For the sake of presentation, it can be assumed that in a given cycle, the memory controllers perform READ operations (FIG. 8) to produce read address before performing WRITE operations (FIG. 8) to obtain the write address. (Emphasis added.)

This passage clearly describes how a FIFO memory can be configured for a dual port memory, while avoiding simultaneous memory access to the same memory location, but does not describe or suggest that the FIFO memory can operate as from one up to a predetermined number greater than one of independent FIFO queues as recited in Claim 21. Also, Kumar Column 24, lines 44-65 states:

> ...Also shown in the FIG. 10 is an [sic] stream of incoming cells input to the example switching apparatus for 8 pipeline cycles. In FIG. 10, input ports of the 4×4 switch are denoted by W,X,Y and Z respectively. Also, the group of cells arriving in eight input cycles are denoted by letter 'A' through 'H'. Each incoming cell is denoted by its output line destination address. For example, the cell arriving in second pipeline cycle on the input port X is destined to the output line '2'. Similarly, the group of cells arriving in second pipeline cycle is denoted by 'B'.
>
> FIG. 11 also shows different pipeline stages of the switching apparatus according to the present invention. Since the switching apparatus is 4×4 and uses 6 memory modules, a 4×6 self-routing and a non-blocking interconnection network is used for pipeline stage 2. Similarly, a 6×4 self-routing and a non-blocking interconnection network is used for pipeline stage 5 in the exemplary embodiment of the disclosed switching system according to this invention. Each memory modules are

> implemented as dual port memory and use the local memory controller for WRITE and READ operations.

This passage describes different configurations of controllers, pipeline cycles, switching apparatus and interconnection networks for ATMs, but does not disclose that a given FIFO memory can be configured to operate as from one up to a predetermined number greater than one of independent FIFO queues, as recited in Claim 21.

Finally, Kumar Columns 28-30 that were cited by the Official Action, are the columns of Kumar's claims. Applicants will not reproduce all of the claims of Kumar here for the sake of brevity. However, these claims also do not appear to describe or suggest the above-quoted recitations of Claim 21. Accordingly, at least the above-underlined recitations of Claim 21 are simply not disclosed in Kumar. Nor would it be obvious to provide a reconfigurable FIFO memory based on the fixed FIFO memory of Kumar. Accordingly, Claim 21, and dependent Claims 22-25 that depend therefrom, are patentable over Kumar.

Applicants also respectfully submit that the Official Action has not established a *prima facie* case of obviousness in rejecting Claims 21-25. In particular, to establish a *prima facie* case of obviousness, three basic criteria must be met. The prior art reference (or references when combined) must teach or suggest *all of* the claim limitations. There must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings, and there must be a reasonable expectation of success of the combination. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found *in the prior art*, not in applicant's disclosure. See MPEP § 2143. As affirmed by the Court of Appeals for the Federal Circuit, to support combining references in a §103 rejection, evidence of a suggestion, teaching, or motivation to combine must be *clear and particular*, and this requirement is not met by merely offering broad, conclusory statements about teachings of references. *In re Dembiczak*, 50 USPQ 2d 1614, 1617 (Fed. Cir. 1999). The Court of Appeals for the Federal Circuit has also stated that, to support combining or modifying references, there must be particular evidence from the prior art as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *In re Kotzab*, 55, USPQ 2d 1313, 1317 (Fed. Cir. 2000).

In discussing the alleged obviousness of Claim 21, the Official Action states at Page 3:

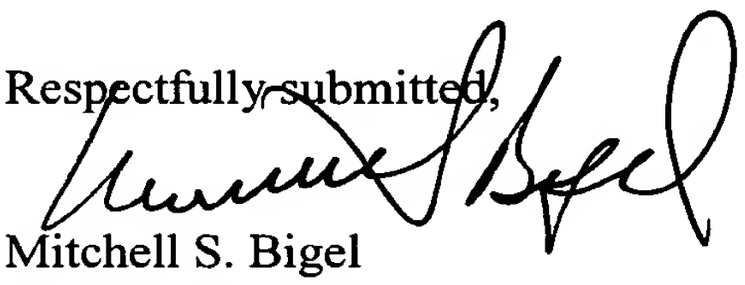
> *Kumar* teaches a packet switch system wherein select incoming packets are routed to independent memory modules. *Kumar* teaches storing one or more parameters in the associated with the incoming packets. Each independent memory modules [sic] each have a corresponding controller that is configured to control access to the respective memory modules. Further, it would have been obvious to one or ordinary skill that the parameter word tags i, k, j are used by each of the controller(s) for determining where to output the stored packets via the memory module(s).

Applicants respectfully submit that this passage does not appear to relate to the recitation of Claim 21 that "a FIFO controller that is configured to operate the FIFO memory as from one up to a predetermined number greater than one of independent FIFO queues". Accordingly, Applicants respectfully submit that a *prima facie* case of obviousness has not been established.

Finally, although Applicants respectfully submit that dependent Claims 22-25 are independently patentable for the reasons that were described in their Request for Reconsideration of July 19, 2004, this analysis will not be repeated for the sake of brevity.

In conclusion, Applicants again appreciate the thorough examination and the Examiner's indication that Claims 1-20 and 28-40 are allowed and that Claims 26 and 27 would be allowable. However, the analysis provided above has shown that Kumar does not appear to describe or suggest the recitations of Claim 21. Accordingly, all of the pending claims are patentable over Kumar and Applicants respectfully request allowance of the present application.

Respectfully submitted,

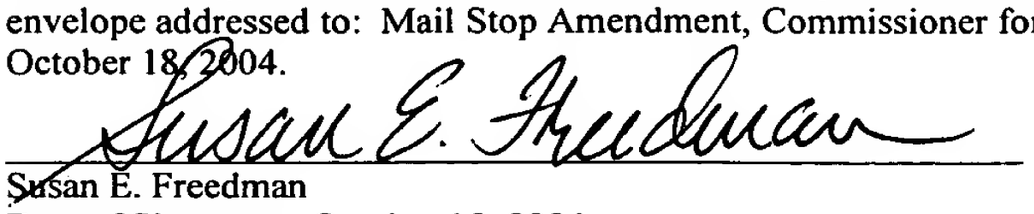


Mitchell S. Bigel
Registration No. 29,614
Attorney for Applicants

Customer Number 20792
Myers Bigel Sibley & Sajovec, P.A.
P.O. Box 37428, Raleigh, NC 27627
919-854-1400
919-854-1401 (Fax)

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 18, 2004.



Susan E. Freedman
Date of Signature: October 18, 2004